

Subject Code: C5803

M.Tech - I Semester [R09] Regular/Supplementary Examinations, April - 2012

**COMPUTER ORGANIZATION and ARCHITECTURE
(Common to CSE and NN)**

Time: 3 Hours

Max Marks: 60

Answer any FIVE questions. All questions carry EQUAL marks.

1. a. Explain about parity checker and parity generator with an example.
b. Why do we use K-maps? What are its applications? Explain.
2. a. What is a decoder? Explain about NAND gate decoder and also explain, how a decoder can be expanded?
b. Define Flip-flop, Explain the construction of SR Flip-flop.
3. Explain about Associative memory with its Hardware organization.
4. a. What is a segment register? List out the Advantages of segmented memory.
b. Explain various types of 8086 instruction formats.
5. Explain the following instructions of 8086
i) TEST AL, BH ii) WAIT iii) XLATB iv) LOCK XCHG BL.
6. Develop an 8086 assembly language program that converts the given Hexadecimal data in to ASCII and vice-versa.
7. With the help of a Flow chart, Explain Booth's multiplication algorithm.
8. Write short notes on the following,
 - a. Serial communication.
 - b. DMA.
 - c. Priority interrupts.

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